CLAIMS

We Claim:

1. An isolated analog-to-digital converter system having at least two channels, said isolated analog-to-digital converter system comprising:

first and second analog-to-digital converters for receiving respective analog input signals and outputting respective digital data signals; and

first and second calibration resistors coupled to the respective outputs of the first and second analog-to-digital converters, for use in calibrating relative gain of the first and second analog-to-digital converters wherein relative gain of the first and second analog-to-digital converters is calibrated from the ratio of the resistances of the first and second calibration resistors.

2. The isolated analog-to-digital converter system of claim 1, wherein the first and second analog-to-digital converters each further include:

an on-chip CMOS bandgap reference calibrated with the matched inputs from the first and second calibration resistors, respectively.

3. The isolated analog-to-digital converter system of claim 2, further comprising:

wherein the first and second calibration resistors comprise a pair of matched precision resistors.

4. The isolated analog-to-digital converter system of claim 3, further comprising:

a data receiving device, coupled to the first and second analog converters, for receiving data from the first and second analog-to-digital converters.

5. The isolated analog-to-digital converter system of claim 4, further comprising:

first and second isolation transformers, each coupled between a respective first and second analog-to-digital converter and the data receiving device, for isolating the data receiving device from the first and second analog-to-digital converters.

6. The isolated analog-to-digital converter system of claim 5, further comprising:

a current limiting/isolating resistor, coupled between the first and second analog-to-digital converters, for limiting overall current and isolate the first and second calibrations resistors from one another.

7. The isolated analog-to-digital converter system of claim 6, wherein the first and second analog-to-digital converters are referenced to respective local grounds GND1 and GND2 having independent potentials.

8. The isolated analog-to-digital converter system of claim 7, wherein the first and second calibration resistors are on a common substrate which has good thermal conduction and electrical insulation characteristics.

9. The isolated analog-to-digital converter system of claim 8, wherein each of the first and second analog-to-digital converters are on respective semiconductor chips, each semiconductor chip provided with silicon thermal meters,

wherein the isolated analog-to-digital converter system is subject to a two-temperature factory calibration.

10. The isolated analog-to-digital converter system of claim 2, wherein

said first and second calibration resistors carry substantially the same current, with the first and second analog-to-digital converters drawing substantially no current from the first and second calibration resistors, such that the first and second calibration resistors provide a pair of ratio matched voltages for the calibration of the CMOS bandgap references in the respective first and second analog-to-digital converters.

11. The isolated analog-to-digital converter system of claim 10, wherein, after initial testing calibration, the gains of the first and second analog-to-digital converters are known, and the first and second analog-to-digital converters measure and record the ratio R1/R2 of the first and second calibration resistors to one another such that in field operation with the ratio of R1/R2 assumed to be unchanged, the first and second analog-to-digital converters measure the ratio R1/R2 and gain of one of the first and second analog-to-digital converters is adjusted to match the other of the first and second analog-to-digital converters.

12. A method of automatically calibrating relative gains of an at least two channel isolated analog-to-digital converter system including first and second analog-to-digital converters for receiving respective analog input signals and outputting respective digital data signals, said method comprising the steps of:

providing first and second calibration resistors coupled to the respective outputs of the first and second analog-to-digital converters, respectively, and

calibrating relative gain of the first and second analog-to-digital converters from the ratio of the resistances of the first and second calibration resistors.

13. The method of claim 12, wherein the first and second analog-to-digital converters each further include respective on-chip CMOS bandgap references, and said step of calibrating relative gain of the first and second analog-to-digital converters comprises the steps of calibrating the respective CMOS bandgap references with matched inputs from the first and second calibration resistors.

14. The method of claim 13, the step of providing first and second calibration resistors further comprises the step of providing a pair of matched precision resistors.

15. The method of claim 14, further comprising the step of:

receiving, in a data receiving device, coupled to the first and second analog converters, data from the first and second analog-to-digital converters.

16. The method of claim 15, further comprising the step of:

isolating the first and second analog-to-digital converters from the data receiving device, using respective first and second isolation transformers coupled between respective first and second analog-to-digital converters and the data receiving device.

17. The method of claim 16, further comprising the step of:

limiting overall current through the first and second calibration resistors and isolating the first and second calibration resistors from one another by providing a current limiting/isolating resistor, coupled between the first and second analog-to-digital converters.

18. The method of claim 17, wherein the first and second analog-to-digital converters are referenced to respective local grounds GND1 and GND2 having independent potentials.

19. The method of claim 18, wherein the step of providing the first and second calibration resistors further comprises the step of providing the first and second calibration resistors on a common substrate which has good thermal conduction and electrical insulation characteristics.

20. The method of claim 19, wherein each of the first and second analog-to-digital converters are on respective semiconductor chips, each semiconductor chip provided with silicon thermal meters, said method further comprising the step of

calibrating the respective gains of the first and second analog-to-digital converters with a two-temperature factory calibration.

21. The method of claim 13, wherein the first and second calibration resistors carry substantially the same current, with

the first and second analog-to-digital converters drawing substantially no current from the first and second calibration resistors, such that the first and second calibration resistors provide a pair of ratio matched voltages for the calibration of the CMOS bandgap references in the respective first and second analog-to-digital converters.

22. The method of claim 21, wherein after initial testing calibration, the gains of the first and second analog-to-digital converters are known, said method further comprising the steps of:

measuring, using the first and second analog-to-digital converters, the ratio R1/R2 of the first and second calibration resistors to one another,

recording, using the first and second analog-to-digital converters, the ratio R1/R2 of the first and second calibration resistors to one another,

measuring, using the first and second analog-to-digital converters, in a subsequent field calibration, assuming the ratio of R1/R2 is unchanged, the ratio R1/R2, and

adjusting the gain of one of the first and second analog-to-digital converters to match the other of the first and second analog-to-digital converters.

23. A power measuring system for measuring power current, comprising:

an isolated analog-to-digital converter system having at least two channels, said isolated analog-to-digital converter system comprising:

first and second analog-to-digital converters for receiving respective analog input signals and outputting respective digital data signals; and

first and second calibration resistors coupled to the respective outputs of the first and second analog-to-digital converters, for use in calibrating relative gain of the first and second analog-to-digital converters wherein relative gain of the first and second analog-to-digital converters is calibrated from the ratio of the resistances of the first and second calibration resistors.

24. The power measuring system of claim 23, wherein the first and second analog-to-digital converters each further include:

an on-chip CMOS bandgap reference calibrated with the matched inputs from the first and second calibration resistors, respectively.

25. The power measuring system of claim 24, further comprising:

wherein the first and second calibration resistors comprise a pair of matched precision resistors.

26. The power measuring system of claim 25, further comprising:

a data receiving device, coupled to the first and second analog converters, for receiving data from the first and second analog-to-digital converters.

27. The power measuring system of claim 26, further comprising:

first and second isolation transformers, each coupled between a respective first and second analog-to-digital converter and the data receiving device, for isolating the data receiving device from the first and second analog-to-digital converters.

28. The power measuring system of claim 27, further comprising:

a current limiting/isolating resistor, coupled between the first and second analog-to-digital converters, for limiting overall current and isolate the first and second calibrations resistors from one another.

29. The power measuring system of claim 28, wherein the first and second analog-to-digital converters are referenced to respective local grounds GND1 and GND2 having independent potentials.

30. The power measuring system of claim 29, wherein the first and second calibration resistors are on a common substrate which has good thermal conduction and electrical insulation characteristics.

31. The power measuring system of claim 30, wherein each of the first and second analog-to-digital converters are on respective semiconductor chips, each semiconductor chip provided with silicon thermal meters,

wherein the isolated analog-to-digital converter system is subject to a two-temperature factory calibration.

32. The power measuring system of claim 24, wherein said first and second calibration resistors carry substantially the same current, with the first and second analog-to-digital converters drawing substantially no current from the first and second calibration resistors, such that the first and second calibration resistors provide a pair of ratio matched voltages for the calibration of the CMOS bandgap references in the respective first and second analog-to-digital converters.

33. The power measuring system of claim 32, wherein, after initial testing calibration, the gains of the first and second analog-to-digital converters are known, and the first and second analog-to-digital converters measure and record the ratio R1/R2 of the first and second calibration resistors to one another such that in field operation with the ratio of R1/R2 assumed to be unchanged, the first and second analog-to-digital converters measure the ratio R1/R2 and gain of one of the first and second analog-to-digital converters is adjusted to match the other of the first and second analog-to-digital converters.